

Q1 detail *infra*). The etch stop layer 130 is deposited having a thickness of approximately 10-100nm. The etch stop layer 130 provides a uniform remaining passivation thickness T' over both the fuse 114A and the alignment mark 142 for use during the subsequent fuse deletion process.

In the Claims

Please cancel claims 5-6. Claims 1-4 and 7-8 are currently pending based on the amendment herein, wherein claim 1 has been amended herein.

Sub B1 Q2 1. (Amended) A semiconductor device comprising:
a substrate,
at least one fuse embedded within an interior portion of the substrate;
a continuous etch resistant layer on a surface of the substrate, wherein the etch resistant layer is directly over the at least one fuse; and
at least one insulative layer above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove.

2. The semiconductor device of claim 1, further comprising an alignment mark formed on the substrate at a location spatially removed from the fuse.

3. The semiconductor device of claim 2, wherein the alignment mark further comprises the etch resistant layer thereover.